Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A digital-to-analog converting circuit comprising:

a first potential terminal for supplying a first potential;

a second potential terminal for supplying a second potential;

an output node for outputting an analog signal;

a first resistor circuit having a plurality of first resistors connected in series between a first node and the output node through a plurality of first connecting points;

a first switching circuit including P-channel type MOS transistors, each of the P-channel type MOS transistors connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only the P-channel type MOS transistors are connected to the first resistors as switches;

a second resistor circuit having a plurality of second resistors connected in series between a second node and the output node through a plurality of second connecting points;

a second switching circuit including N-channel type MOS transistors, each of the N-channel type MOS transistors connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node, wherein

only the N-channel type MOS transistors are connected to the second resistors as switches; and

a control circuit connected to the first and second switching circuits for controlling the P-channel type MOS transistors and the N-channel type MOS transistors,

wherein the control circuit concurrently turns off all of the p-channel type MOS transistors and all of the N-channel type MOS transistors responsive to an externally applied control signal, and

wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 2 (Canceled)

Claim 3 (Previously Presented): A digital-to-analog converting circuit according to claim 1, wherein the second switching circuit further has an N-channel type MOS transistor connected between the second potential terminal and the output node.

Claim 4 (Canceled)

Claim 5 (Previously Presented): A digital-to-analog converting circuit according to claim 1, wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistors and a second decoder for controlling the N-channel type MOS

transistors.

Claim 6 (Canceled)

Claim 7 (Original): A digital-to-analog converting circuit according to claim 1, further comprising an amplifier connected to the output node for amplifying the analog signal.

Claim 8 (Currently Amended): A digital-to-analog converting circuit comprising:

a first potential terminal supplying a first potential;

a second potential terminal supplying a second potential;

an output node providing an analog signal;

a plurality of first resistors connected in series between a first node and the output node, the first resistors being connected to each other at a plurality of first connecting points;

a plurality of first switches each of which is connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only P-channel type MOS transistors are connected to the first resistors as switches;

a plurality of second resistors connected in series between a second node and the output node, the second resistors being connected to each other at a plurality of second connecting points;

a plurality of second switches each of which is connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node, wherein only N-channel type MOS transistors are connected to the second resistors as switches; and

a control circuit connected to control the P-channel type MOS transistors and the N-channel type MOS transistors,

the control circuit including a plurality of NAND gates that provide respective control signals to the P-channel type and N-channel type MOS transistors responsive to externally provided bit signals, and that concurrently disable all of the P-channel type and N-channel type MOS transistors responsive to an externally provided disable signal,

wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 9 (Canceled)

Claim 10 (Previously Presented): A digital-to-analog converting circuit according to claim 8, further comprising an additional N-channel type MOS transistor connected between the second potential terminal and the output node.

Claim 11 (Canceled)

Claim 12 (Previously Presented): A digital-to-analog converting circuit according to claim 8, wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistors and a second decoder for controlling the N-channel type MOS transistors.

Claim 13 (Canceled)

Claim 14 (Original): A digital-to-analog converting circuit according to claim 8, further comprising an amplifier connected to the output node for amplifying the analog signal.

Claims 15-21 (Canceled)

Claim 22 (Previously Presented): A digital-to-analog converting circuit comprising:

a first potential terminal ~~for supplying~~ that supplies a first potential;

a second potential terminal ~~for supplying~~ that supplies a second potential;

an output node ~~for outputting~~ that outputs an analog signal;

a first resistor circuit having a plurality of first resistors connected in series between a first node and the output node through a plurality of first connecting points;

a first switching circuit including P-channel type MOS transistors, each of the P-channel type MOS transistors connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only the P-

channel type MOS transistors are connected to the first resistors as switches;

a second resistor circuit having a plurality of second resistors connected in series between a second node and the output node through a plurality of second connecting points;

a second switching circuit including N-channel type MOS transistors, each of the N-channel type MOS transistors connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node, wherein only the N-channel type MOS transistors are connected to the second resistors as switches; and

a control circuit connected to the first and second switching circuits [[for]] that selectively turns ~~turning~~ on only one of the P-channel type MOS transistors and one of the N-channel type MOS transistors at a time[[,]] to provide the analog signal at the output node, and that concurrently turns off all of the P-channel type MOS transistors and all of the N-channel type MOS transistors responsive to an externally provided disable signal.

Claim 23 (Previously Presented): A digital-to-analog converting circuit according to claim 22, wherein the second switching circuit further has an N-channel type MOS transistor connected between the second potential terminal and the output node.

Claim 24 (Previously Presented): A digital-to-analog converting circuit according to claim 22, wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistors and a second decoder for controlling the N-channel type MOS transistors.

Claim 25 (Previously Presented): A digital-to-analog converting circuit according to claim 22, wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 26 (Previously Presented): A digital-to-analog converting circuit according to claim 22, further comprising an amplifier connected to the output node for amplifying the analog signal.